

A self-aligned nano-fabrication process for vertical NbN–MgO–NbN Josephson junctions

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We present a new process for fabricating vertical NbN–MgO–NbN Josephson junctions using self-aligned silicon nitride spacers. It allows for a wide range of junction areas from $0.02\ \mu\text{m}^2$ to several $100\ \mu\text{m}^2$. At the same time, it is suited for the implementation of complex microwave circuits with transmission line impedances ranging from $< 1\ \Omega$ to $> 1\ \text{k}\Omega$. The constituent thin films and the finished junctions are characterized. The latter are shown to have high gap voltages ($> 4\ \text{mV}$) and low sub-gap leakage currents.

I. INTRODUCTION

Josephson junctions (JJ) are the key nonlinear element used in superconducting circuits^{1–3}. In applications where large critical currents are needed, typically Nb–Al₂O₃–Nb, NbN–MgO–NbN or NbN–TaN–NbN junctions are used. This is the case for superconducting quantum interference device (SQUID) magnetometers³, Josephson mixers⁴ or rapid single flux quantum (RSFQ) logic circuits⁵. The high critical temperature and large superconducting gap of Nb and NbN enable these devices to operate at liquid helium temperatures (4K) and up to very high frequencies (above 1 THz for NbN). Such junctions are typically fabricated by first depositing the junction stack and then etching a pillar from it. The main difficulty is to contact the top of this pillar without short-circuiting it to the bottom layer. Common solutions to this problem, such as an additional insulating layer that is etched away above the pillar or anodic oxidation of Nb usually limit the minimum junction area to approximately $1\ \mu\text{m}^2$ ^{6–9}. This results in high critical currents and large shunting capacitances.

However, certain superconducting quantum circuits, such as Josephson qubits and Josephson photonic devices, require these quantities to be small. Because of this, it is much more common to use Al–Al₂O₃–Al junctions, which can be fabricated using shadow angle evaporation; a technique allowing for very small Josephson junction sizes down to $0.01\ \mu\text{m}^2$ or less^{10,11}. The downside of this approach is that the low gap of Aluminum sets an ultimate limit for the fabricated devices in operation frequency (below 100 GHz) as well as temperature.

Here, we report on a fabrication process able to simultaneously obtain NbN–MgO–NbN junctions with surface areas as small as $0.02\ \mu\text{m}^2$ and as large as several $100\ \mu\text{m}^2$. This marks an important step towards bringing the advantages of NbN–MgO–NbN junctions to quantum circuits that were so far limited to Al junctions and opens the possibility for such circuits to operate at much higher frequencies. It is particularly useful for the field of Josephson photonics^{12–16}, which requires small junctions and could provide devices like quantum microwave sources and amplifiers able to function up to the gap frequency of the superconductor.

The presented NbN junction fabrication process also

enables us to implement very versatile passive microwave circuits at no extra cost. The large kinetic inductance of NbN can be used to design high impedance circuit elements, which are useful for many quantum circuits in general and Josephson photonics in particular.

II. FABRICATION OF JOSEPHSON JUNCTIONS

The NbN thin films are prepared by DC magnetron sputtering on Si(500 μm):SiO₂(500 nm) substrates. After cleaning the wafers by back-sputtering in the deposition chamber, a 20 nm magnesium oxide (MgO) buffer layer is added as etch stop and to improve the superconducting properties of the NbN film. This is followed by the deposition of an NbN(10 nm):MgO(4 nm):NbN(190 nm) stack (hereafter called the trilayer)¹⁷. The NbN is DC magnetron sputtered from an Nb target in an atmosphere of Ar and N₂ (see supplementary information for detailed process parameters). Scanning electron microscope images of cuts through the produced NbN films show them to be columnar with an average column diameter of $\approx 20\ \text{nm}$.

The aspect ratio imposed by the thickness of the deposited layers and the lateral junction sizes calls for very directional etch processes. We have developed several dry etch recipes on an Oxford ICP Plasmalab100 reactive ion etcher. During the etch, NbN is attacked both chemically, with SF₆, as well as mechanically with Ar. A moderate platen power generates an auto-polarization voltage of $\approx 190\ \text{V}$ accelerating the ions towards the sample and makes the etch more directional. Moreover, CH₂F₂ is added to the mixture, with the effect of polymerizing the exposed surface of the NbN film, making it less sensitive to the chemical etch. While in the vertical direction the Ar bombardment constantly ablates the polymer film and leaves the surface exposed to the chemical etch, the sidewalls of steps and trenches stay protected, preventing any underetch and assure smooth and steep sidewalls (see Fig. 1).

The MgO-barrier is etched purely mechanically with an argon plasma. MgO is insensitive to the NbN etch described above, allowing us to use the buffer and barrier layers as effective etch stops, despite their very small thickness. Consequently the NbN etch can run longer

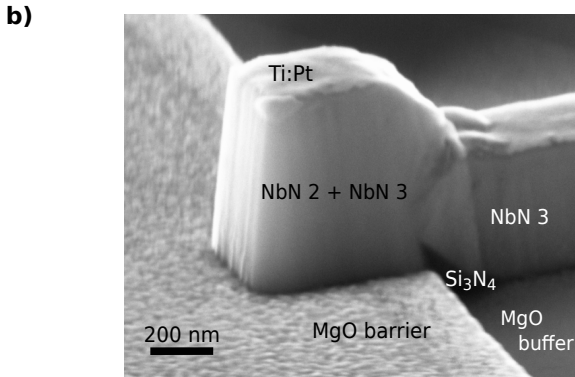
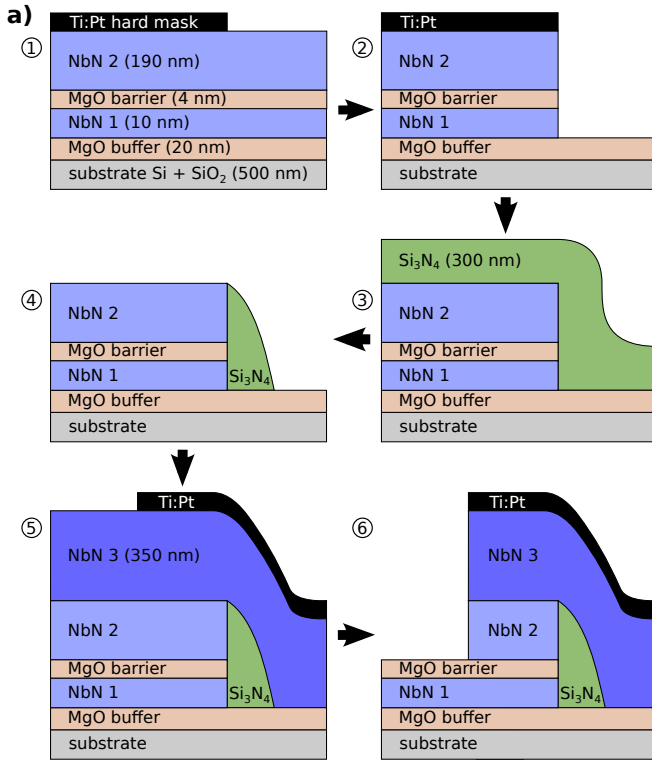


Figure 1. Sample fabrication: (a) The different steps of the fabrication process. First the NbN-MgO-NbN trilayer is sputtered (1) and etched (2) using a Ti:Pt hard mask. Then a dielectric layer is deposited conformally by chemical vapor deposition (3) and etched directionally (using a Ti:Pt hard mask) to leave spacers passivating the trilayer sidewalls (4). Finally a counter electrode layer is deposited (5) and etched down to the junction barrier (6). (b) Finished $150\text{ nm} \times 150\text{ nm}$ junction defined by EBL with a Ti:Pt hard mask still in place.

to counteract inhomogeneities in deposition and etching rate across the wafer.

During the entire fabrication process described below optical lithography (OL) and electron beam lithography (EBL) steps are combined in order to be able to define small structures with high precision, while keeping the processing times for bigger structures such as coplanar waveguide (CPW) transmission lines¹⁸ low. The following description will, however, focus on the elaboration of a single small Josephson junction and thus disregards some of the OL steps.

To begin with, a step is etched into the trilayer using

an EBL defined Ti(10 nm):Pt(60 nm) hard-mask (Fig. 1), which is subsequently removed with an Ar plasma. Next, the entire wafer is coated with a 300 nm thick film of Si_3N_4 by chemical vapor deposition. A 10 nm thick layer of MgO is deposited on top of the SiN in order to protect it from overetching during some of the following fabrication steps. An optical lithography step is carried out defining regions where the dielectric will be etched. The entire junction lies in such an area. First, the MgO in these areas is removed by a dip in 1% acetic acid. We then perform a directional dry-etch of the SiN, similar to the one developed for NbN. The vertical thickness of the dielectric at the step is considerably bigger than elsewhere. Hence, it can be etched away on all flat surfaces while leaving behind a self-aligned spacer protecting the side of the trilayer (Fig. 1).

Finally, after a back-sputtering step, the NbN counter-electrode ($\approx 350\text{ nm}$) is deposited. Another EBL defined hard-mask protects an area in the shape of a finger overlapping with the step. Once the unprotected areas are etched down all the way to the MgO tunneling barrier, this finger forms the vertical Josephson junction shown in Fig. 1 (see supplementary material for details of the etch recipes).

III. SIMULTANEOUS IMPLEMENTATION OF PASSIVE ELEMENTS

The fabrication steps used to implement the junction enable us to simultaneously fabricate very versatile passive microwave circuits on the same chip. In particular, the process allows for various types of transmission lines: A line defined in the counter-electrode layer on top of the SiN forms a microstrip line together with the ground plane given by the trilayer. This case is ideal for low-impedance transmission lines (we estimate $65\ \Omega$ for $1\ \mu\text{m}$ wide lines, down to $< 1\ \Omega$ for $100\ \mu\text{m}$ wide lines). However, these impedances depend critically on the exact dielectric thickness and, because of high kinetic inductance fractions around 0.8, on the NbN material properties. Coplanar wave guide (CPW) geometries using the full thickness of the trilayer can be tuned for transmission line impedances between $20\ \Omega$ and $150\ \Omega$ ¹⁶. This impedance and propagation speed are accurately controlled by lateral geometry because kinetic inductance fractions are low (< 0.25 except for extreme geometries) and the substrate dielectric constant is well known. For even higher impedances, the dielectric on top of the CPW center conductor can be removed before the counter-electrode etch step. As a result, the upper part of the trilayer is etched away during this step, thinning down the center conductor to 10 nm like in the junction area (see Fig. 1). For such thin layers the NbN kinetic inductance is dominating and leads to characteristic impedances of up to $3.5\ \text{k}\Omega$ for a $1\ \mu\text{m}$ wide wire. In areas where the SiN dielectric layer is not etched, it separates the trilayer and the counter-electrode, allowing for straightforward implementation of parallel plate capacitors. Where needed, holes can be etched in the dielectric to provide vias connecting the two layers. This enables us to fabricate crossovers between the ground planes of the CPW

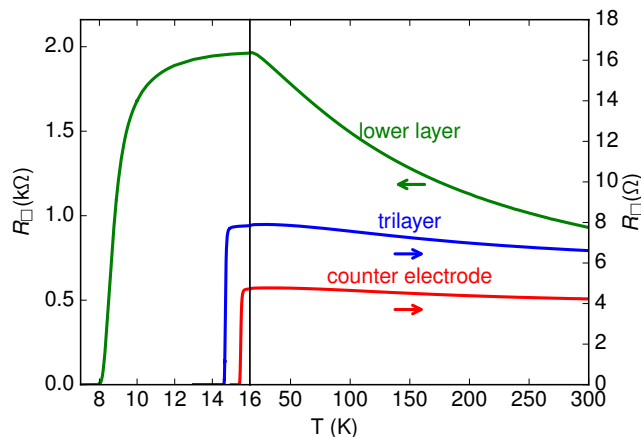


Figure 2. Square resistance as a function of temperature for the different layers of our process. Arrows indicate on which resistance scale the data is plotted. The temperature curves of lower, trilayer and counter electrode layers give a critical temperature of respectively 8.8, 14.7 and 15.5 K and we estimate their surface inductances $L_{\text{kin},\square}$ to be, respectively, 300, 0.81, 0.55 pH.

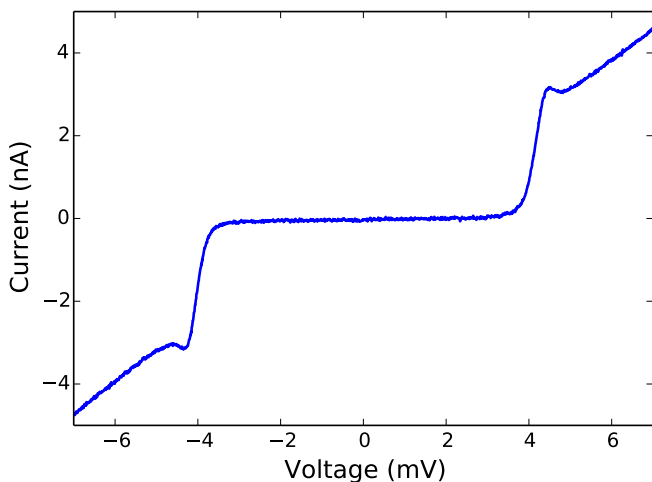


Figure 3. Typical current voltage characteristics. The curve shows the data for a SQUID consisting of two parallel Josephson junctions with dimensions of 150 nm \times 150 nm.

transmission lines, thus effectively eliminating parasitic modes^{19–22}.

IV. PROPERTIES OF THE FABRICATED FILMS AND JUNCTIONS

Temperature dependent resistance measurements of the deposited layers were performed in a commercial physical property measurement system (PPMS) (see Fig. 2).

We calculate the value of the kinetic inductance $L_{\text{kin},\square}$ from the square resistances R_{\square} (taken at 20 K) of the film, its thickness d and the superconducting gap Δ estimated from the critical temperature, according to^{23,24} $L_{\text{kin},\square} = \mu_0 \lambda \coth(d/\lambda)$. Here $\lambda = (\hbar R_{\square} d / (\mu_0 \pi \Delta))^{1/2}$

is the London penetration depth of a local superconductor in the low temperature limit $k_B T \ll \Delta$ ^{25,26}. For the bottom layer $d \ll \lambda$ so that $L_{\text{kin},\square} \approx \hbar R_{\square} / (\pi \Delta)$ can be estimated without knowing the exact film thickness.

A typical current-voltage characteristic of a superconducting interference device (SQUID) consisting of two parallel junctions with a total area of 0.04 μm^2 (squares of 150 nm side-length) measured at 4.2 K is shown in Fig. 3. The gap voltage V_{gap} can be defined as the voltage at the steepest part of the curve, where dI/dV is maximized²⁷. Here, $V_{\text{gap}} = 4.15$ mV corresponding to an emission frequency of ≈ 1 THz in the framework of Josephson photonics^{12,16,28}. A normal state resistance $R_N \approx 1.5$ M Ω can be extracted from the same curve far above V_{gap} at 7 mV. Together with the Ambegaokar-Baratoff formula at zero temperature²⁹ $I_c R_N = \pi \Delta(0) / 2e$ and the relation $2\Delta = eV_{\text{gap}}$ we can evaluate the theoretical critical current at zero temperature to be ≈ 2.2 nA. The critical current density is ≈ 5.5 A cm^{-2} . Note that, even though our junctions are optimized for low critical current densities, J_c can easily be increased by several orders of magnitude with this deposition process¹⁷. The current branch of the IV in Fig. 3 is not visible, because the associated energy scale²⁹ $E_J = \Phi_0 I_c / (2\pi) \approx 4.5$ μeV , where Φ_0 is the magnetic flux quantum, is much smaller than the thermal energy at 4.2 K ($k_B T \approx 360$ μeV). The "knee" in the current-voltage characteristic is usually associated with the formation of a thin normal metal close to the junction barrier and has frequently been observed in NbN–MgO–NbN Josephson junctions^{30–32}. In the context of this work we took particular interest in minimizing the leakage current under the gap¹⁶. In order to quantify the subgap leakage we compare the resistance under the gap (R_S) at 3 mV to R_N . A linear fit of the current voltage characteristic in Fig 3 between -3 mV and 3 mV gives $R_S \approx 80$ M Ω leading to $R_N/R_S < 0.02$. While the measured gap voltage on this specific sample is lower than the best values reported in the literature, the subgap resistance is comparable to the numbers achieved in other groups^{27,32,33}. In particular, it should be pointed out that the smallest NbN–MgO–NbN tunnel junctions found in the literature have surface areas around 0.1 μm^2 , several times bigger than the junction presented here, while showing considerably more subgap leakage^{27,34,35}.

V. POSSIBLE VARIATIONS

The current process is not suitable for applications requiring resonators with very high quality factors, such as circuit QED. CPW resonators realized with this process¹⁶ typically have intrinsic quality factors of 10^4 . We attribute this low value to dielectric loss in the MgO and SiO₂ buffer layers. We expect a significant increase of this value by omitting the MgO buffer layers and using sapphire substrates instead. The latter allow to directly grow high quality NbN films without buffer layer and provide a good etch stop. If transmission lines with higher impedances are needed, the thickness of the lower NbN layer can be reduced. Replacing the silicon sub-

strate with a silica substrate, increases the characteristic impedances of CPWs by another factor ~ 1.7 .

If high kinetic inductance is not desired, the process, with slight adjustments, should be applicable also to Nb-(Al)-Al₂O₃-Nb trilayers, where the barrier is formed by oxidizing a thin proximized aluminum layer. We expect that such a process yields lower leakage current below the gap because of the more uniform self-passivating barrier.

The current density is voluntarily kept low for the application in mind¹⁶, but can be increased by several orders of magnitude by decreasing the thickness of the MgO barrier layer¹⁷.

Finally, if only larger junction sizes are needed, the junctions can exclusively be defined by optical lithography, considerably reducing fabrication times. In this case, the geometry is changed so that a counter-electrode wire crosses a trilayer wire. This makes the junction size insensitive to slight misalignments between the two optical lithography steps.

VI. CONCLUSION

In conclusion, we have developed a new fabrication process for vertical NbN–MgO–NbN Josephson with self-aligned SiN spacers allowing for very small junction areas. The measured junction current–voltage characteristics show a high gap voltage and to our knowledge the lowest subgap leakage current at these junction sizes reported so far. The process allows for simultaneous fabrication of very large Josephson junctions and extremely versatile passive microwave circuits with characteristic impedances ranging from $< 1\ \Omega$ to $> 1\ \text{k}\Omega$.

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SUPPLEMENTARY MATERIAL: DETAILED PROCESS PARAMETERS

A. Film deposition

NbN and MgO films are deposited in an Alcatel SCM600 sputter tool. The NbN–MgO–NbN trilayer is deposited *in situ* without exposing the sample to air between steps. Substrates are not actively heated, but their temperature increases above ambient temperature during the process.

NbN films prepared by reactive DC magnetron sputtered from a 150 mm Niobium target at 4 A and $\approx 400\ \text{V}$

in an atmosphere of 1.5 Pa of Ar and 0.2 Pa of N₂. The latter partially nitrates the target surface after the target surface has been conditioned in an atmosphere containing more nitrogen. The deposition rate is $\approx 3.3\ \text{nm s}^{-1}$. For very thin layers we rotate the sample stage over different targets at $\approx 0.6\ \text{Hz}$ reducing the average deposition rate by approximately a factor 7 for a more precise control of thickness.

The MgO barrier is RF magnetron sputtered at 450 W in an Ar atmosphere at 1.3 Pa for 100 s, in the same chamber as the NbN films, also with rotating sample. For deposition of the buffer layer we increase power to 550 W, keep the sample on top of the target and use an atmosphere of 1.25 Pa of Ar and 0.1 Pa of N₂.

Si₃N₄ is deposited in a Corial D250L plasma enhanced chemical vapor deposition (PECVD) tool at 280 °C and 200 W at a pressure of 200 Pa with flows of 100 SCCM of SiH₄, 500 SCCM of NH₃ and 100 SCCM of Ar.

B. Etch parameters

Tables I, II, III give details on our etch recipes in an Oxford Plasmalab 100 ICP etcher. The different rows of each table correspond to the steps followed chronologically during the procedure. Landing steps are performed to homogenize the NbN etch over the entire wafer and are possible because MgO provides a very good etch stop. Values in parentheses are used to start the plasma and then quickly ramped down to the regular parameters. The purely mechanical MgO etch steps are interleaved with pumping and venting of the process chamber in order to evacuate excess material. EPD stand for “end point detection”, which is performed using *in situ* laser reflectometry.

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	CH ₂ F ₂ (SCCM)	SF ₆ (SCCM)	Ar (SCCM)	Pressure (mTorr)	ICP (W)	Forward (W)	Time (s)
upper NbN	25	5	40	5(15)	500	70	EPD
NbN landing	10	10	40	20	500	20	15
4×	MgO		100	5	500	150	20
	Pump			0			150
	Vent			atmospheric pressure			90
lower NbN	25	5	40	5(15)	500	70	EPD
NbN landing	10	10	40	20	500	20	15

Table I. Procedure of etching the trilayer and counter electrode. Thin lower layers (below approximately 30 nm) are transparent and allow for end point detection in the first step. If thicker lower layers are required, the first etch has to be timed instead. For the final etch of the counter electrode (and upper part of the trilayer, see paper) the etch is stopped before the MgO step.

	CH ₂ F ₂ (SCCM)	SF ₆ (SCCM)	Ar (SCCM)	Pressure (mTorr)	ICP (W)	Forward (W)	Time (s)
Si ₃ N ₄	25	5	40	5(15)	(1000,500),250	(150),50	EPD

Table II. Procedure for etching Si₃N₄ dielectric. Before this etch the MgO cap layer is removed by dipping the wafer in 1% acetic acid for 20s.

	O ₂ (SCCM)	Pressure (mTorr)	ICP (W)	Forward (W)	Time (s)
O ₂ plasma	45	30	500	0	300

Table III. Etch for removing resist residues after etching and stripping.

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